13. (Currently Amended) The method of claim 12, further comprising, a storage capacitor including first capacitor electrode and a second capacitor electrodes with a dielectric layer interposed therebetween, the first capacitor electrode extending from either of the source electrode and the drain electrodes and including the pixel electrode material layer and the metal material layer, each stacked sequentially, the second capacitor electrode including a gate electrode material layer, the dielectric layer electrode formed on the first capacitor electrode and including the capping insulating layer and the first insulating layer, each stacked sequentially.

14. (Original) The method of claim 13, further comprising, forming a contact hole contemporaneously with forming the pixel electrode having the opening portion, the contact hole contacting the first capacitor electrode and the gate electrode.

15. (Added) The method of claim 10, wherein the first source electrode directly contacts the first end portion of the semiconductor layer and the second source electrode directly contacts the second end portion of the semiconductor layer.

16. (Added) The method of claim 10, wherein the first insulting layer is formed over an entire surface of the insulating substrate.

17. (Added) The method of claim 10, wherein the high-density source region directly contacts the source electrode and the high-density drain region directly contacts the drain electrode.

IN THE SPECIFICATION:

A marked-up copy of the changes to selected paragraph(s) is provided below.

Please insert the following paragraph on page 1, between lines 4 and 5:

This application is a divisional application of and claims priority to co-pending U.S. Patent Application No.10/120,425, which is incorporated herein in its entirety.

Please replace the originally filed paragraph with the amended paragraph(s), as shown below. Please amend the paragraph on page 8, line 22 – page 9, line 9, as follows:

Subsequently, referring now to FIGs. 3D and 4, a second insulating layer is deposited over the entire surface of the transparent substrate 110 and is anisotropically etched to form a first spacer 250 on side wall portions of the source and drain electrodes 170 and 175 an d on the side wall portion of the source and drain electrodes 235 and 236, respectively. Thereafter, a second ion-implanting process is performed: a high-density impurity having an opposite conductivity to that of the first ion-implanting process (i.e., n+-type impurity) is ion-implanted into the exposed portions of the semiconductor layers 160 and 210. As a result, the central portions 166 and 216 of the semiconductor layers 160 and 210 enter a non-ion doped state and thus serve as a channel area. Also, both end portions of the semiconductor layers 160 and 210, under the source and drain electrodes 170, 175, 235, and 236 and the first spacer 250, serve as high-density source and drain regions 161, 162, 211, and 212.

IN THE DRAWINGS:

Attached hereto is a replacement drawing for FIG. 3D, without any markings. FIG. 3d is amended to correctly recite reference numeral '211' instead of reference numeral '214'. The Examiner is requested to acknowledge consideration of the changes to the drawings.